Foundation IP for High-Performance Computing Designs on TSMC N7 FinFET Process

Synopsys



ABSTRACT

TSMC's new N7 FinFET process provides inherent power and area advantages, which will soon make it the preferred node for SoCs targeting applications including automotive, mobile, and high-performance computing.

SoC designers using this process can make the most of the process's features when combined with a Foundation IP portfolio of logic libraries and memory compilers that can take advantage of these unique process features.

This presentation will describe how Synopsys has closely aligned with TSMC's extensive ecosystem and latest PDKs and to deliver a range of Foundation IP to meet specific customer application requirements using the most advanced EDA tool flows. The Foundation IP specialized for TSMC's process enables designers to maximize processing capability and minimize power in computing and networking applications, meet high automotive reliability and achieve ultra-low dynamic and leakage power in mobile. Designers can combine the advantages of the TSMC N7 process with Synopsys' portfolio of logic libraries, embedded memories with test and repair, as well as interface IP, to achieve their application's performance, power, area and reliability targets.

SYNOPSYS
Silicon to Software

Foundation IP for High-Performance Computing Designs on TSMC N7 FinFET Process

Ken Brock, Logic Libraries Product Marketing Manager, Synopsys

September 13, 2017

Agenda

High Performance Computing with N7

N7 Impact on CPUs/GPUs

Foundation IP PPA Optimization

Summary

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Markets Driving N7 Adoption

- The **first wave designs** are either:
 - Very high volume to justify the increased cost of N7
 - **Very high margin product to justify the increased ROI of N7**
- The **first wave designers** value:
 - The ability to pack much more functionality on a die
 - The power reduction from the migration to N7
 - The significant performance increase due to N7
- The **markets** that are justifying early adoption of N7:
 - Mobile - Smartphones & tablets
 - **Server CPUs, GPUs & high-performance computing (HPC)**
 - Enterprise networking
 - **Automotive ADAS**



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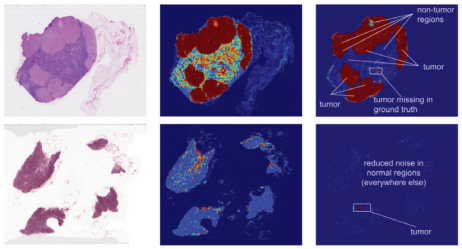
Medical Applications Powered by HPC and AI

Health Research Efforts of the Brain Team at Google

Detecting Diabetic Eye Disease



Detecting Cancer



Source: Google

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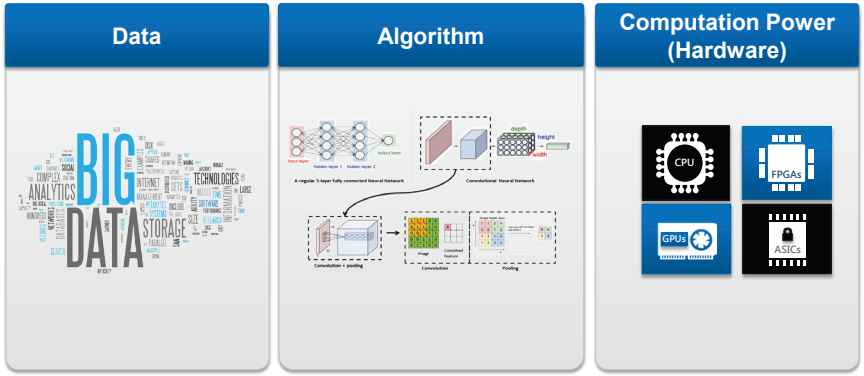
Automotive Applications Powered by HPC and AI

ADAS Image Recognition and Deep Learning

- Pedestrian detection
- Autonomous driving
- Sign recognition
- Object detection

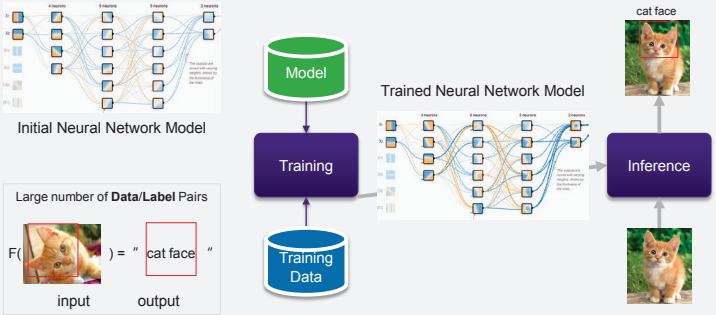


Three Keys to the Rise of Deep Learning



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Deep Learning Framework



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Is N7 Right for Your HPC SoC?

- **Readiness**
 - How ready is the process?
 - Is the ecosystem ready?
- **Performance**
 - Can you achieve the performance you need?
 - Does the performance create new possibilities?
- **Power**
 - Leakage power
 - Dynamic power
- **Area**
 - What is the area reduction needed for cost?
 - Does this enable more transistors for additional functionality, smaller die for cost?
- **Implementation**
 - Do you have access to all of the expertise you need to deliver this design on schedule?
- **Reliability and Yield**
 - How manufacturable is your design in this process, at first tapeout and when you will be in volume production?

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N7 Process Enables GPUs & CPUs for HPC

- **GPU**
 - Hundreds of simpler cores
 - Thousands of concurrent hardware threads
 - Maximizing floating-point throughput
 - Most die surface for integer and FP units
 - Lower speed, low voltage (CFV^2), variability

- Higher current per fin enables 60% power reduction at same speed in HD cell
- 60% area scaling enables increased functionality on economic die

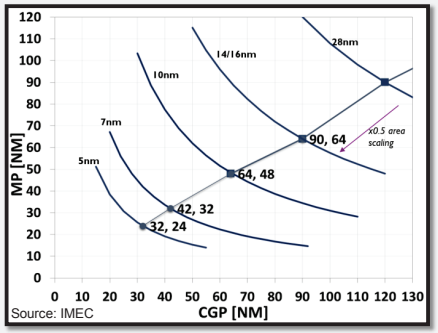
- **CPU + Accelerators**
 - Very few complex cores
 - Single thread performance optimization
 - Transistor space dedicated to complex ILP
 - Little die surface for integer and FP units
 - Higher speed, power distribution, EM

- Performance improvement of 35% at constant power in HS cell is key reason to move to N7
- IP is optimized for highest performance and robust power grids

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Fin Depopulation Benefits in Area/Power Scaling

Lower Fin-count Becoming More Focused in 7nm



- **Further area scaling**
 → Lower number of Fins achieve target speed

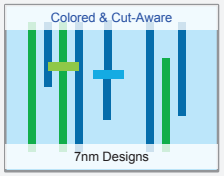
- **Lower dynamic power**
 → Smaller number of Fins reduce dynamic power

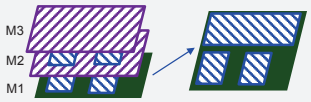
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Area – N7 Layout Design Challenges

- Cut metal utilized on routing layers
 - Cut metal rules and cut metal functions
 - Region dependent design rule requirements
- Increase of restricted design rules
- The lowest-layer metals only go in one direction
- No wide wires – via ladders for performance/EM
- Integration with advanced EDA tools







Standard cell areas have different design rule within a layer

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High Performance Computing with N7

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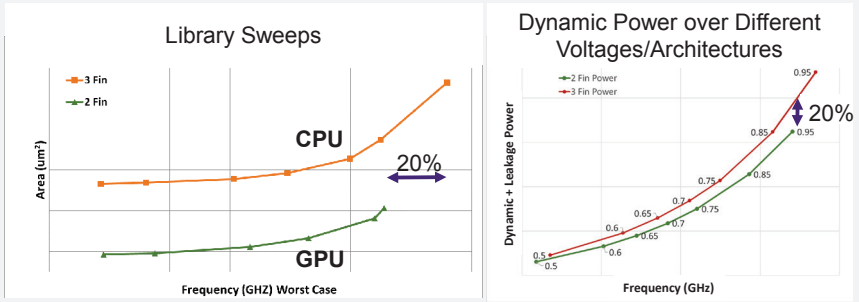
Foundation IP PPA Optimization

Summary

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Cell Architectures Enable PPA Tradeoffs on N7

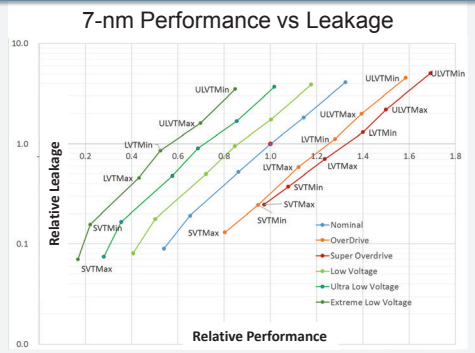
DesignWare Logic Library Architecture



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Wide Voltage Range Enables Power/Performance Tradeoffs

DesignWare Logic Library Architecture



- PVT corners at nominal voltages & multiple overdrive & underdrive groups support designs from the highest performance to lowest power
- Lower voltages for power optimization
 - –Performance of SVT degrades at low voltages
 - –Variability increases at extreme low voltages
- LVF is standard to manage variability

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Embedded Memory PPA Options

DesignWare Embedded Memories

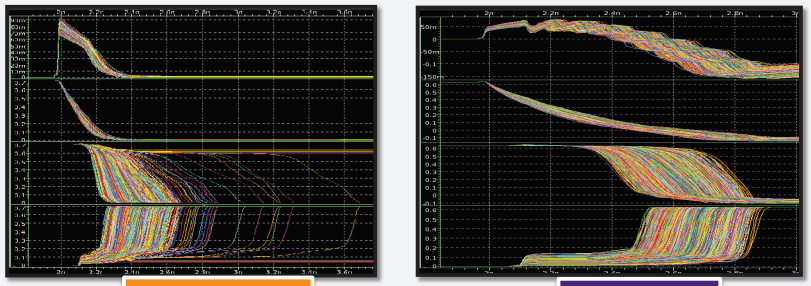
Periphery Design	Bitcell Choice	Periphery Design	Bitcell Choice
Area		Performance	
Aspect Ratio (Mux, Banks)	Center Decode, Test & Repair	Periphery Vt Device	Read & Write Margin
Clock Gating	R/W Assist for Low Voltage	Sleep Modes	Periphery Vt Device
Dynamic Power		Leakage	
Dynamic Voltage Scaling	Dual Rail	Channel Length	Architecture

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Low Voltage Operation: Use of Assist

DesignWare Embedded Memories

• N7 memory compilers support read, write assist to enable lower Vmin



Without Write Assist | With Write Assist

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HPC Design Kit Component Summary

Suite of HS & HD Memories & Logic Libraries to Optimize GPUs/CPUs/DSPs

Component	CPU	GPU	DSP	Primary Benefit
Logic Library				
High-Speed Flops	●		●	Critical path performance
Area-optimized Flops		●	●	Register area
Multi-bit Flops		● ●	● ●	Dynamic power/Area savings
Metastable-optimized Flops	● ●	● ●	● ●	Reliable synchronizers
Combinational Cells		●	●	Minimize routing congestion
Memory				
Fast Cache Instances (Popular CPUs, GPUs, DSPs)	●		●	Critical path performance
UHD 2 Port RF Compiler		● ●		Reduces area and leakage
High-Density Single Port Instances		● ●	● ●	Reduces area and power

NOTE: Pre-optimized RM+flow scripts and core optimization services also available

Optimized for: ● Performance ● Power ● Area

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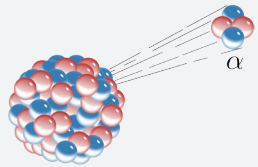
Foundation IP to Support Advanced N7 Design Flows

FinFET grid Even site width/height rule Color aware PG routing Macro alignment & pin snapping Cut-metal route-guide and grid	NDM Library	Color aware library support Cut-metal aware library support
	Synthesis & Test	Via ladder support in synthesis Timing, area correlation to ICC II
Advanced timing modeling Variation Tolerance Clock EM Dynamic power	Design Planning Place_opt	Advance layer rule (Vt/OD/TPO) PG & pin-density aware placement Pin color alignment, pin access awareness Layer-aware, track RC
Advanced rule aware filler/decap insertion Cut-Cut-metal aware, colored data output Advanced ECO In-Design DRC In-Design metal fill	Clock_opt Route_opt	Metal extn, cut-metal, color aware rule Advanced correlation Wire optimization Signal EM POCV Colored extraction
Via ladder support through the flow from lib prep, place_opt, CTS, Clock_opt, Route_opt to Finishing and Signoff	Finishing	

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TSMC's N7 Manufacturability & Reliability

- 7nm process is stabilizing at TSMC faster than earlier nodes
 - Impressive SRAM defect densities (D0)
- Synopsys IP development is progressing for TSMC N7 and its variants
- Different 7nm-specific SRAM failure mechanisms
 - Synopsys' STAR Memory System has new 7nm specific algorithms to catch and repair these faults
 - Memories also need row redundancy to handle the smaller geometries
- Aging needs to be addressed for HCI, PTBI, NBTI, with TDDB
- Developing multiple SER optimized designs for 7nm



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Building on 2016 Collaboration Announcement with TSMC

Joint Efforts Resulted in Multiple N7 Tapeouts of Logic Libraries, Embedded Memories & Interface IP


News Release

Synopsys and TSMC Collaborate on Development of Interface and Foundation IP for 7-nm FinFET Process

Joint Efforts Result in Multiple 7-nm Customer Tapeouts of DesignWare Logic Libraries and Embedded Memories

MOUNTAIN VIEW, Calif., Sept. 19, 2016 (PRNewswire) --

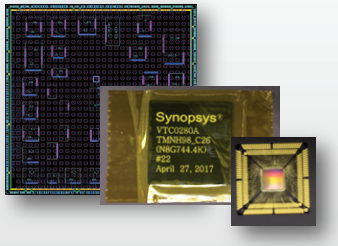
Highlights:

- Successful customer tapeouts of Synopsys DesignWare Logic Libraries and Embedded Memories on 7-nm demonstrates high quality and reduces integration risk
- Integrated Synopsys STAR Memory System solution enables efficient test and repair of 7-nm memories
- Early development of IP enables first wave of 7-nm designs targeting mobile and high-performance computing applications
- DesignWare Interface IP in development for TSMC 7-nm process includes USB, PCI Express, DDR, MIPI, DisplayPort, SATA and Ethernet

Synopsys, Inc. (Nasdaq: SNPS) today announced the successful tapeout of multiple customer test chips with DesignWare® Logic Libraries and Embedded Memories for TSMC's 7-nanometer (nm) FinFET process. The tapeouts mark a significant milestone in Synopsys' and TSMC's collaboration on the development of DesignWare Logic Library, Embedded Memory and Interface IP for TSMC's 7-nm FinFET process. The collaboration extends Synopsys' long history of successful IP development for TSMC advanced

"Achieving multiple customer tapeouts of Synopsys DesignWare IP on TSMC's 7nm process demonstrates the benefits of our collaboration and gives designers confidence that they will **meet their power, performance and area targets**."

Suk Lee, TSMC senior director



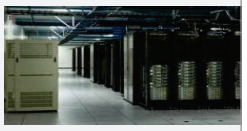
Fully Functional N7 Testchip

Synopsys N7 Foundation IP Differentiations

Superior PPA and Proven expertise in HPC, Automotive

- Highly Manufactureable IP
 - Synopsys TCAD-based DTCO ensures best manufacturability
 - Best-in-class silicon validation methodologies
 - Highest volume Foundation IP (FIP) in TSMC 16nm (>500K wafers)
- Superior PPA
 - Synopsys FIP delivers industry leading PPA through close interaction with DCG/ICC2/PT
- Automotive expertise
 - ASIL D Ready FIP at TSMC 16nm certified by SGS-TUV
 - Automotive Grade 1

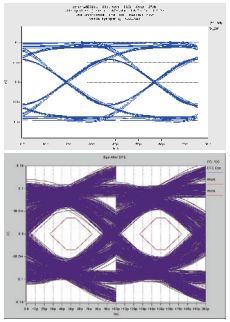






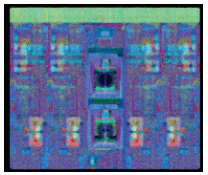
DesignWare Interface IP Eye Diagrams and Test Chips on TSMC N7

- Simulated Eye Diagrams

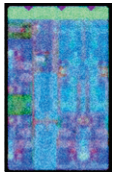


- 25G Settings
 - no EQ
 - boost code = 15
- USB 3.1 TX eye with reference channel, AFE, and DFE

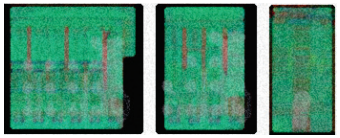
- Test Chips



25G x4 with PMA



USB 3.1 w/DP x4



MIPI 4xTX, 2xRX with PLL

Synopsys is Ready for Your N7 Design

- Achieve optimal N7 PPA compared to 16nm
 - 60% smaller area
 - 35% higher speed at same power level
 - 60% power reduction at same speed
- Synopsys has expertise building IP at N7 for several HPC customers
 - Multiple N7 Foundation & Interface IP tapeouts
- Synopsys Foundation IP and Interface IP accelerates TTM and maximizes QOR

Synopsys IP Portfolio for N7

- Taped out
 - Logic Libraries
 - HPC Design Kits
 - PCI Express® 4.0/3.1
 - DDR4
 - SATA 6G
 - Embedded Memories
 - USB 3.1/2.0
 - DisplayPort 1.4
 - Ethernet
- In development
 - LPDDR4x
 - HBM2
 - MIPI M-PHY
 - MIPI D-PHY